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FULLY REUSED VLSI ARCHITECTURE OF DSRC ENCODERS USING SOLS TECHNIQUE

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ABSTRACT

Dedicated short-range communications (DSRC) are one-way or two-way from short-range to medium-range wireless communication channels specifically designed to push the intelligent transportation system into our daily life. The DSRC standard generally uses FM0 and Manchester codes which to reach dc-balance, enhancing the signal reliability. Generally the code word structure of FM0 encoding and Manchester encoding are different, thus limiting the hardware potential of existing DSRC systems. In this paper, the Finite State Machine (FSM) of FM0 code is constructed and from the FSM, the architecture of FM0 encoding is developed and then the combine hardware architecture of FMO and Manchester encoding is constructed.

KEYWORDS: In DSRC, FSM, FM0, Manchester.

INTRODUCTION

DSRC communication implemented fundamentally on standards based on interoperability among devices from different manufacturers. The dedicated short-range communication is a technique for one- or two-way medium range communication especially used for intelligent transportation systems. The DSRC can be briefly divided into two parts i.e. vehicle-to-vehicle and vehicle-to- roadside. In vehicle-to-vehicle, the DSRC activated the message sending and broadcasting among vehicle for safety issues and public information announcement. The Safety issues consist of blind-spot, intersection warning, intercars distance, and collision-alarm. The vehicle-to-roadside focuses on the intelligent transportation service, such as automatic electronic toll collection (ETC) system. With electronic toll collection, the toll collecting is electrically or automatically accomplished with the contactless IC-card platform. Moreover, the electronic toll collection has application such as payment for parking-service, and gas-refueling. Thus, the DSRC plays an important role in automobile industry. Generally, the Waveform of transmitted signal is expected to have zero mean for robustness noise, and this is also called as dc-balance. The transmitted signal consists of arbitrary binary sequence, (1 or 0) which is difficult to achieve dc-balance. The goal of FM0 and Manchester codes can provide the transmitted signal with dc-balance. Both FM0 and Manchester codes are widely designated in encoding for downlink.

The system architecture of DSRC transceiver is shown in Fig 1.

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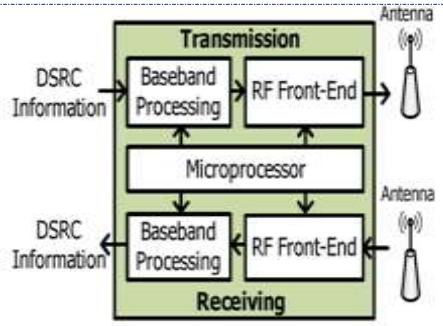

Fig. 1: System architecture of DSRC transceiver

The upper and bottom parts are designed for transmission and receiving, respectively. This transceiver is partitioned into three basic modules: microprocessor, baseband processing and RF front-end. The microprocessor takes and manipulates the instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is dedicated for encoding, error correction, clock synchronization, and modulation. The RF front-end transmits and receives the wireless signal from antenna for communication.

LITERATURE SURVEY

In last few years VLSI architecture of Manchester encoder is used in optical communications [1]. A new Manchester code generator designed at transistor level is represented. This Manchester code generator uses 32 transistors and has the same complexity as a standard D flip-flop.

The VLSI architecture of Manchester encoder [2] further replaces the architecture of switch in [1] by the NMOS device. It is realized in 90-nm CMOS technology, and its maximum clock frequency is as high as 5 GHz. The high-speed VLSI architecture also fully reused with Manchester and Miller encodings [3] for radio frequency identification (RFID) applications is implemented. This design is realized in 0.35-µm CMOS technology and has the maximum operation frequency is 200 MHz.This design uses concept of parallel operation to improve data throughput. In addition, the technique of hardware sharing is improved in this design to reduce the number of transistors. This design uses TSMC CMOS 0.35-µm 2P4M technology. A Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator [4] is designed. This hardware architecture is constructed from the finite state machine (FSM) of Manchester code, and is implemented into field-programmable gate array (FPGA) prototyping system. The similar design methodology is further applied to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator [5].Its maximum operating frequency is about 192 MHZ. Furthermore,[6] combines frequency shift keying (FSK) modulation and demodulation with Manchester codec in hardware realization.

RELATED WORK

In this part, the clock signal and the input data are denoted as CLK and X. with this parameters the coding principles of FM0 and Manchester codes are explained as follows.

(i).FM0 Encoding

As given in Fig 2, for each X, the FM0 code structure consists of two parts: one for former-half cycle of CLK, A, and the other one for later-half cycle of CLK, B.

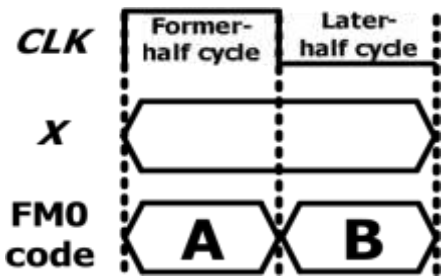

Fig.2:Codeword structure of FM0.

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The coding principle ofFM0 is listed as the following three rules.

1) If X is the logic-0, the FM0 code must exhibit a transition between A and B
2) If X is the logic-1, no transition is allowed between A and B.
3) The transition is allocated among each FM0Code no matter what the X is.

Fig.3 shows the waveform of FM0 encoding.

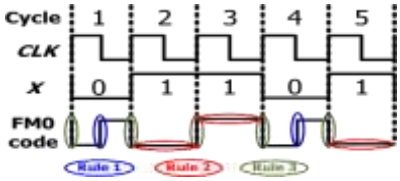
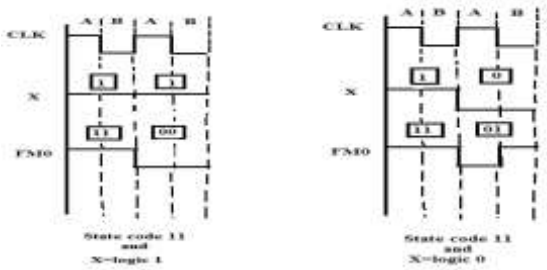


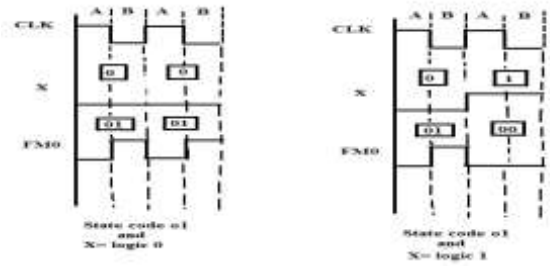
Fig.3:Illustration of FM0 coding

As shown in fig 4, for each X, FM0 has two parts. if state code is 11 and X=logic 1 then next state for FM0 is 00 and if state code is 11 and X=logic o then next state for FM0 is 01.



(a) ***(b)***

Fig 4: Waveform for State code 11

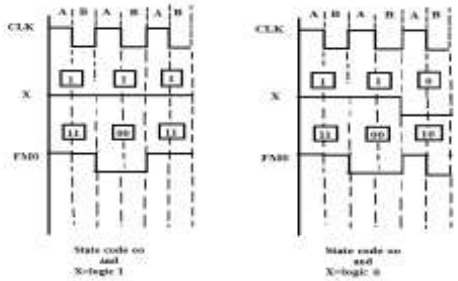


(a) ***(b)***

Fig .5: Waveform for State code 01

As shown in fig 5, for each X, FM0 has two parts. if state code is 01 and X=logic 0 then next state for FM0 is 01 and if state code is 01 and X=logic 1 then next state for FM0 is 00.

As shown in fig 6, for each X, FM0 has two parts. if state code is 00 and X=logic 1 then next state for FM0 is 11 and if state code is 00 and X=logic 0 then next state for FM0 is 10.



(a) ***(b)***

Fig 6: Waveform for State code 00

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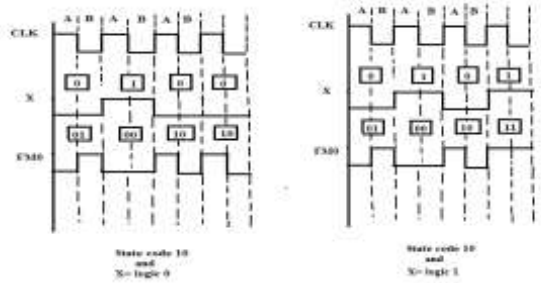
As shown in fig 7, for each X, FM0 has two parts. if state code is 10 and X=logic 0 then next state for FM0 is 10 and if state code is 10 and X=logic 1 then next state for FM0 is 11.



(a) ***(b)***

Fig 7: Waveform for State code 10

(ii).Manchester Encoding

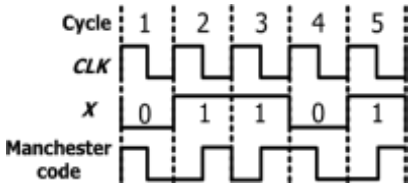


Fig 8: Illustration of Manchester coding example

The Manchester coding example is shown in Fig. 8. The Manchester code is obtained from

$$X \oplus CLK. \qquad (1)$$

The Manchester encoding is designed with a XOR operation for X and CLK. The clock always has always transition within one cycle, and so does the Manchester code no matter what the *X* is.

HARDWARE ARCHITECTURE OF FM0 AND MANCHESTER ENCODERS

The hardware architecture of Manchester encoding is as simple as a XOR operation. However, the construction of hardware architecture for FM0 is not as simple as that of Manchester encoding. The hardware architecture of FM0 encoding is constructed with the help of FSM of FM0 with the help of fig.4, 5,6,7. As shown in Fig. 9(a), the FSM of FM0 code is divided into four states. A state code is individually given to each state, and each state code having a value of A and B, as shown in Fig. 2. According to the coding principle of FM0, the FSM of FM0 coding is shown in Fig. 9(b). Suppose the initial state is S_1, and its state code is 11 for A and B, respectively. Suppose S_1 is 11, then if X = logic 0 then next state for S_1 is S_3 i.e. 01 and X = logic 1 then next state for S_1 is S_4 i.e. 00.So, the state-transition for each state can be completely constructed.

The FSM of FM0 coding can also conduct the transition table of each state, as given in Table II. A(t)and B(t)denotes the discrete-time state code of current-state at time instant *t*. Their previous-states are represent as the A(t− 1) and the B(t− 1), respectively. With the help of transition table, the Boolean functions of A (t) and B (t) are given as follows:

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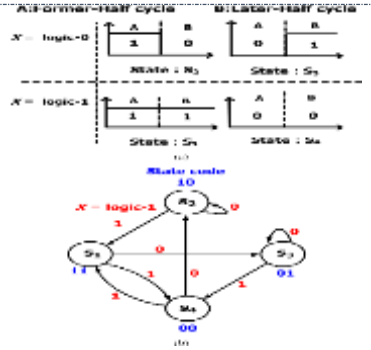

Fig 9:Illustaration of FSM for FMO (a)States definition (b)FSM of FM0 coding.

$$A(t)= \overline{B(t-1)} \quad (2)$$

$$B(t)= X \oplus B(t-1) \quad (3)$$

With both A(t)and B(t), the Boolean function of FM0 code is represent as

$$CLK\ A(t) + \overline{CLK}\ B(t) \quad (4)$$

With (1) and (4), the hardware architectures of FM0 and Manchester encoders are given in Fig.10

The top part is denoted for the FM0 code and the bottom part is denoted for the Manchester code. In FM0 code the DFF_A and DFF_B are used to store the state code of the FM0 code and also MUX-1 and not gate is used in the FM0 code. The Manchester code is developed only using the XOR gate. The MUX−1 is used to switch A(t)and B(t) through the selection of CLK signal. Both A(t)and B(t)are driven by (2) and (3), respectively. The determination of which coding is used depends on the Mode selection of the MUX−2.when the mode=0 is assign for the FM0 code and when the mode=1 is for the Manchester code. The hardware utilization rate is defined as the following:

$$HUR=\frac{Activecomponents}{TotalComponents} \times 100\% \quad (5)$$

TABLE 1. TRANSITION TABLE FOR FM0 ENCODING

Previous-state		Current-state			
		$A(t)$		$B(t)$	
$A(t-1)$	$B(t-1)$	$X=0$	$X=1$	$X=0$	$X=1$
1	1	0	0	1	0
1	0	1	1	0	1
0	1	0	0	1	0
0	0	1	1	0	1

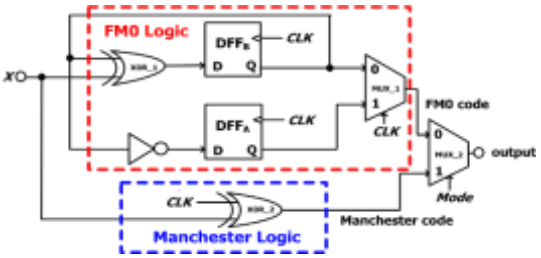

Fig 10:Hardware architecture of FM0 and Manchester encodings

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The active components means the components are work in the FM0 or Manchester code. The total components means the number of the components are present in entire hardware architecture. For both the encoding techniques the total components is 7.For the FM0 code active component is 6 and in the Manchester code active component is 2. So Hardware utilization rate is 57.14%.

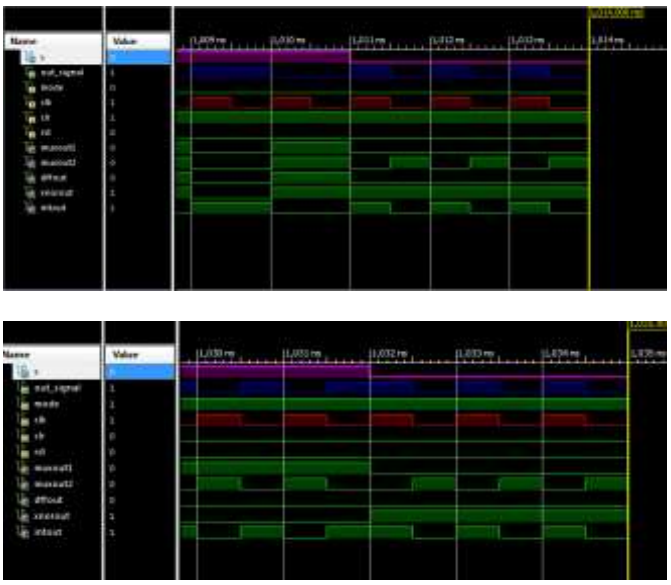

Fig.11:(From top to bottom):Waveform for FM0 encoding, Manchester Encoding

CONCLUSION

In this report the hardware architecture of FM0 and Manchester coding is design using the FSM and transition table. In this design hardware utilization rate is determined.so the HUR is 57.14%.

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